Keypad-Programmable Reference Voltage Generation for DC-DC Converters Using Arduino-PWM: Proteus Simulation and Filter Optimization

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Abstract: This study presents the design and simulation of a microcontroller-based programmable reference voltage system for DC-DC converters using a Proteus simulation environment. The proposed system combines an Arduino UNO virtual model with a 4×4 keypad interface and 16×2 LCD display to generate precision reference voltages through PWM-to-analog conversion. The Proteus implementation features: (1) accurate modeling of Timer1 10-bit PWM generation at 31.25 kHz, (2) SPICE-based simulation of the two-stage RC low-pass filter (1kΩ/10µF → 1kΩ/100nF), and (3) interactive virtual instrumentation for performance validation. Simulation results demonstrate the system's capability to produce stable reference voltages from 0V to 5.00V with 4.88 mV resolution. Virtual oscilloscope measurements show the filtered PWM output achieves <1.5% voltage ripple (p-p) when loaded with a 10kΩ impedance, with settling times of 70 ms for 0V→5V transitions. The Proteus model verifies the effectiveness of the digital control algorithm, including keypad debouncing (modeled with 50ms delay blocks) and dynamic PWM updates without voltage discontinuities. Comparative analysis between ideal mathematical models and Proteus simulations reveals a less than 3% deviation in output voltage accuracy across the operating range. The virtual testing environment enabled the optimization of filter components, demonstrating that increasing the second-stage capacitor to 100nF reduces ripple by 32% while maintaining acceptable settling characteristics. System response to simulated load transients (20%-80% step changes) confirms reference voltage stability within ±1% of setpoint. This work validates the feasibility of the design through comprehensive virtual prototyping, providing a cost-effective simulation framework for developing programmable reference systems before hardware implementation. The Proteus model serves as a versatile testbed for evaluating different filter configurations and control algorithms in power electronics applications.

Keywords: PWM voltage reference, DC-DC converter control, Arduino-PWM, Proteus simulation, RC filter optimization, Programmable voltage generation, 10-bit PWM resolution, Low-cost reference design, Mixed-mode simulation, Second-order filtering

1. INTRODUCTION

Precise voltage reference generation is critical for optimizing DC-DC converter performance in applications ranging from renewable energy systems to portable electronics. Pulse Width Modulation (PWM), a fundamental power electronics technique, enables efficient power regulation by modulating pulse widths to encode control functions, achieving precise system-level regulation (Santra, 2018; Yu, 2022). While commercial voltage reference ICs offer integrated solutions (Tsividis, 1978; Nissinen, 2004; Kinget, 2008) their fixed resolution and high cost often limit flexibility for research and prototyping. Microcontroller-based PWM implementations present a cost-effective alternative (Nallusamy,2023), but they face inherent challenges in maintaining stable analog outputs with low ripple and fast dynamic response. Traditional methods such as resistor dividers and potentiometers (Butyrlagin, 2021; Laszlo, 2014) lack programmability, while dedicated digital-to-analog converters (DACs) introduce unnecessary complexity and cost for many applications.

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This work bridges these gaps by introducing a simulation-validated, Arduino-PWM-based reference voltage system, designed through Proteus co-simulation to enable precise DC-DC converter control without costly hardware iterations. The core challenge in PWM-based reference design lies in balancing competing performance metrics—particularly ripple attenuation versus settling time.

Prior studies have explored PWM-to-analog conversion using microcontrollers (Cherian, 2015; Chariag, 2020) but most lack a unified simulation framework that integrates digital control logic with analog circuit behavior. This work advances the field by introducing a simulation-first methodology using Proteus mixed-mode modeling, enabling precise virtual prototyping of a keypad-programmable reference voltage system for DC-DC converters.

Our research advances the field through three key contributions:

1. A mixed-mode Proteus simulation framework that models the complete signal chain—from Arduino firmware generating 10-bit PWM signals (31.25 kHz) to optimized two-stage RC filtering—enabling virtual prototyping with SPICE-level accuracy.
2. Quantitative analysis of second-order filter trade-offs, demonstrating a 32% ripple reduction (achieved with a 100nF second-stage capacitor) while maintaining sub-70ms settling times.
3. A cost-effective open-design framework that reduces development costs by ~40% compared to commercial solutions while achieving <3% output error across the 0–5V range with 4.88 mV resolution, validated entirely in simulation.

Unlike conventional designs that rely on empirical tuning or fixed filter configurations, this approach provides a **versatile virtual testbed** for evaluating control algorithms and analog performance metrics. The keypad-LCD interface adds user programmability, making the system suitable for educational labs and low-resource prototyping environments.

By combining digital control and analog circuit simulation in a unified environment, this work provides researchers with a practical tool for the rapid development of programmable voltage references, addressing a critical need in power electronics prototyping. This systematic exploration of microcontroller-based reference design through simulation-first methodology offers valuable insights for both academic researchers and power electronics engineers developing adjustable power systems.

The paper is organized as follows: Section 2 details the system methodology including PWM generation mathematics and filter design equations. Section 3 presents Proteus simulation results and discussions analyzing PWM performance and second-order RC filter response. Conclusions and future research directions are given in Section 4.

2. METHODOLOGY

The research methodology encompassed three key phases: system design, Proteus and MATLAB simulation design, and performance validation design.

2.1 System Architecture

In a research paper, system architecture typically describes the structure, components, and interactions within a system. It defines how different elements—such as hardware, software, data, and processes.

2.2 Hardware Component

The hardware component is designed in Proteus Design Suite 8.6. The main components are: 1) Arduino Uno microcontroller, 2) 4x4 keypad, 3) 16x2 LCD, and a filter circuit. The control circuit and the filter circuit are shown in Figure 1.

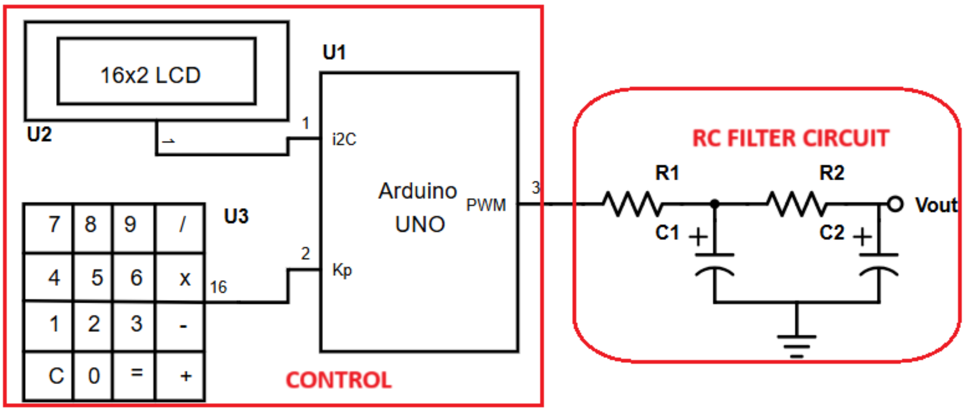

Fig 1.Overview of the control and filtering circuit of the DC-DC proposed converter

Table 1 List of main components and their function used in the proposed work

Component	Functions
Arduino UNO (ATMega328P)	For programmable PWM generation
4x4 Matrix Keypad	For selecting reference voltage input
1602 LCD (i^2C)	For display of input voltage and reference voltage setting
Two-stage RC low-pass filter	Improves attenuation and smooth output signal

3. SIGNAL FLOW

The signal flow diagram in Figure 2 represents a programmable reference voltage control system for a DC-DC converter. The keypad allows users to input the desired reference voltage. The Arduino processes these inputs and converts them into a corresponding PWM signal. The PWM signal is then sent to an RC filter, which smooths it into a stable DC voltage. This filtered voltage serves as the reference input for the DC-DC converter.

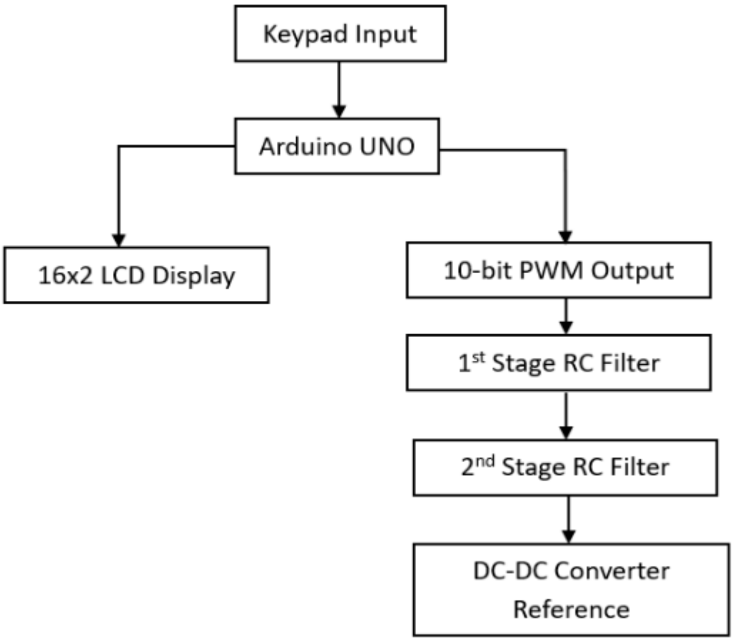

Fig 1. Signal flow of the keypad-programmable DC-DC converter

The converter adjusts its output voltage based on this reference, ensuring precise control. The RC filter design is crucial for minimizing ripple and maintaining accuracy. This setup provides an efficient, microcontroller-based solution for dynamic voltage control in power electronics applications.

3.1 PWM Generation

In DC-DC converters, fixed-frequency, fixed-duty-cycle PWM is commonly employed for open-loop configurations, typically operating within the 20 kHz to 100 kHz range (Santra, 2018). The voltage-PWM relationship can be computed in Equation 1. The Timer1 configuration uses the 10-bit fast PWM mode (TCCR1A/B register settings). The frequency is 31.25kHz (no prescaling, 16MHz clock from Arduino UNO).

$$V_{ref} = \frac{D}{1023} \times V_{\beta} \tag{1}$$

where,
V_{ref} = voltage reference
$D = d$uty cycle $(0 < \mathrm{D} < 1)$
V_{β} = voltage Arduino (usually +5V)

The duty cycle of the circuit is also derived from the voltage difference between the input and output while the circuit is in operation (Ramadhan, 2019).
The theoretical voltage step is given as in equation 2.

$$\mathrm{V_{step}} = \frac{\mathrm{V_{max}}}{\gamma} \tag{2}$$

where,
$\mathrm{V_{step}}$ = theoretical voltage step
$\mathrm{V_{max}}$ = maximum voltage of the converter 5V
γ = mircrontroller resolution (10 − bits)

The Arduino UNO has a 10-bit ADC resolution, therefore, equation 3 computes the voltage step.

$$\mathrm{V_{step}} = \frac{5\mathrm{V}}{1023} \approx 4.88\mathrm{mV} \tag{3}$$

The relationship between equation (1) and (2) achieved maximum 5V converter output at duty cycle of 1.

3.2 Filter Design and Analysis

The RC filter design is composed of two parts: the first stage and the second stage. The filter analysis is a crucial component in reducing output voltage attenuation.

3.2.1 First-order RC Transfer Function

For the first stage RC filter, the transfer function and cut-off frequency are given by equations 4 and 5 respectively as

$$\mathrm{H(s)} = \frac{1}{1 + \mathrm{sRC}} \tag{4}$$

$$\mathrm{f_{c1}} = \frac{1}{2\pi \mathrm{R_1 C_1}} \tag{5}$$

The $R_1 = 1k\Omega$ and $C_1 = 10uF$ for the resistor and capacitor of the first stage filter. The cut-off frequency of the first stage filter is calculated in Equation 6.

$$\mathrm{f_{c1}} = \frac{1}{2\pi \mathrm{R_1 C_1}} \approx 15.9\mathrm{Hz} \qquad (6)$$

3.2.2 Second Stage Filter Optimization

The main purpose of the cascaded filters is to improve ripple attenuation. The formula for voltage ripple is given in equation 7.

$$V_{ripple} = V_{DD} \times \left(1 - e^{-\left(\frac{T_{on}}{RC}\right)}\right) \times e^{-\left(\frac{T_{off}}{RC}\right)} \qquad (7)$$

where,
$T_{on} = D \times T_{PWM}$
$T_{off} = (1 - D) \times T_{PWM}$
$T_{PWM} = 31.25\ KHz = 32us$

The T_{on} and T_{off} is the turn-on and turn-off time of the converter. The D is the duty cycle and T_{PWM} is the frequency of the converter.

3.2.3 Total Filter Response

The total filter response is now given in Equation 8. The output voltage is therefore expected to have reduced attenuation as compared to the first-stage filter.

$$\mathrm{V_{out}} = \mathrm{V_{ref}} \times \left(1 - \mathrm{e}^{-\left(\frac{t}{\tau_1}\right)}\right) \times \left(1 - \mathrm{e}^{-\left(\frac{t}{\tau_2}\right)}\right) \qquad (8)$$

where time constants,

$\tau_1 = \mathrm{R_1 C_1} = (1\mathrm{k}\Omega)(10\mathrm{uF}) = 10\mathrm{ms}$
$\tau_2 = \mathrm{R_2 C_2} = (1\mathrm{k}\Omega)(100\mathrm{nF}) = 0.1\mathrm{ms}$

The voltage ripple reduction in equation 9 can be computed as for a 50% duty cycle:

$$\mathrm{V_{ripple}} \approx \frac{5\mathrm{V} \times \mathrm{T_{PWM}}}{2\mathrm{R_2 C_2}} \qquad (9)$$

Considering the influence of parametric uncertainties, external disturbances, and nonlinear unmodeled dynamics, which impact the control effectiveness of DC-DC converters (Mituletu, 2021). Thus, it is crucial to achieve stability of a system through precise analysis.

3.3 Simulation Setup

The simulation setup is comprised of two simulation methods. The Proteus PWM generation and second order RC filter response, and the MATLAB Simulink focusing on the transient and filter optimization.

3.3.1 Proteus Simulation Setup

The complete system was modeled in Proteus ISIS using mixed-mode simulation, incorporating the Arduino firmware (compiled to .hex), ATMega328P microcontroller model, and SPICE-based analog components with parasitic effects enabled. Simulation protocols included time-domain analysis (transient response, settling time), frequency sweeps, and FFT verification of harmonic attenuation.

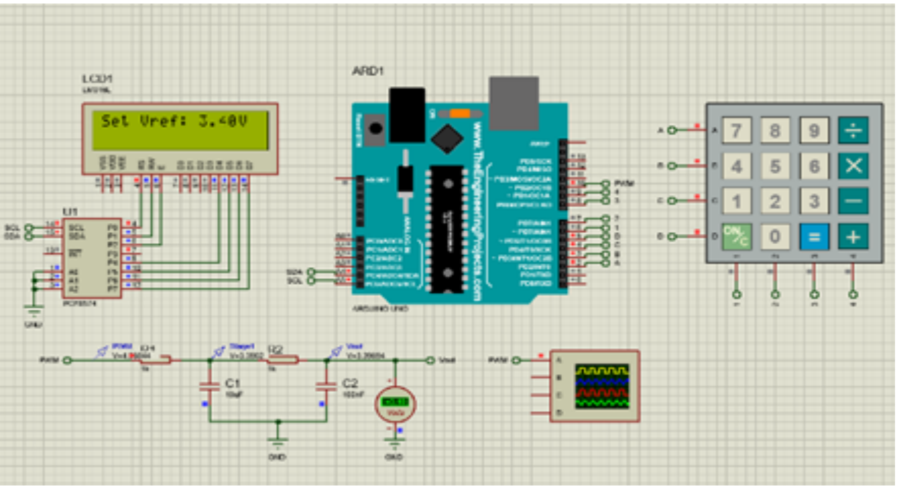

Fig 2. Proteus simulation setup of the keypad-programmable voltage reference DC-DC converter

The Arduino microcontroller is a single-board, open-source hardware system programmed in C, featuring built-in software with a compiler and bootloader, simplifying the generation of PWM triggering signals (Nallusamy, 2023).

4. MATLAB SIMULATION SETUP

The MATLAB simulation setup is used to validate the performance of the second-order filter. The version of the software is MATLAB R2024b.

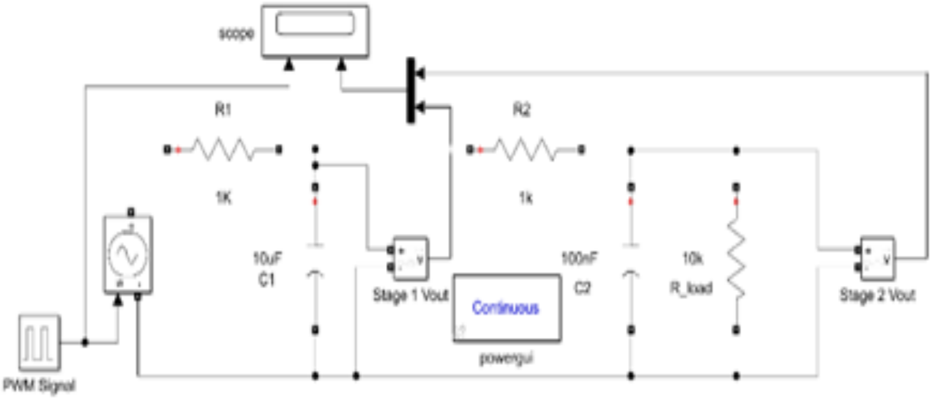

Fig 3. Second-order RC filter design in MATLAB Simulink

Sections 3.2, 3.3, and 3.4 of the results section are generated using the MATLAB. The performance of the filter circuits is analyzed by varying the duty cycle of the PWM signal (Ramadhan, 2019).

4.1 Performance Metrics

Performance metrics were quantitatively evaluated against theoretical models, particularly for ripple voltage. Parameter optimization was conducted through iterative simulations, systematically varying filter components while monitoring output stability under simulated load transients (10kΩ). The virtual testing environment allowed simultaneous observation of digital control signals (PWM duty cycle) and analog outputs, enabling precise correlation between firmware behavior and circuit response.

Table 2 Performance metrics with target parametric metric.

Metric	Formula/Target
Ripple Voltage	$V_{ripple} < 2\%$ of V_{ref}
Settling Time	$\tau_s << 100$ ms
Accuracy Error	$er = \frac{V_{sim} - V_{set}}{V_{set}} \times 100\% < 3\%$

Generating a PWM signal with timers requires one timer for frequency control and another for duty cycle adjustment, utilizing interrupts to reduce CPU load while consuming two timer resources [2]. The target performance is highlighted in Table 2. The settling time is expected to annotate 90% of the final value.

5. RESULTS AND DISCUSSION

In the results section, we will compare the following observations of the simulation; PWM Generation Performance in section 3.1, Transient Response in section 3.2, Filter Optimization Analysis in section 3.3, and System Level Validation in section 3.4

5.1 PWM Generation Performance

The PWM generation performance indicates the relationship between the Arduino UNO PWM output and the response of the DC-DC converter. The results are generated from the Proteus simulation setup in Figure 3 under no-load conditions.

The PWM waveforms in Figures 5, 6, 7, and 8 for duty cycles 0.3, 0.5, 0.8, and 0.98 respectively are observed using the Proteus virtual oscilloscope.

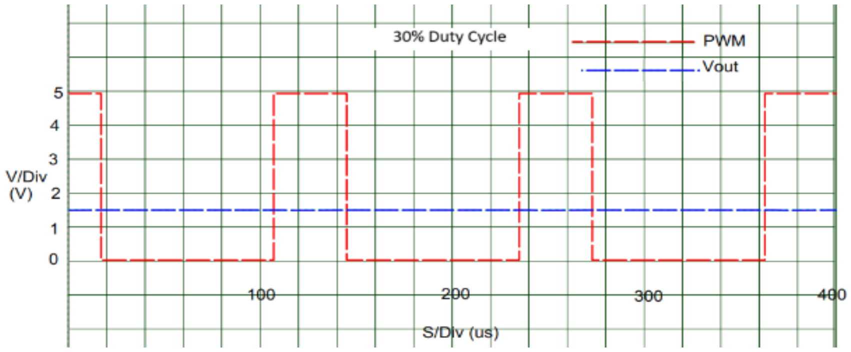

Fig 4. The PWM and the response of the simulation at 30% duty cycle.

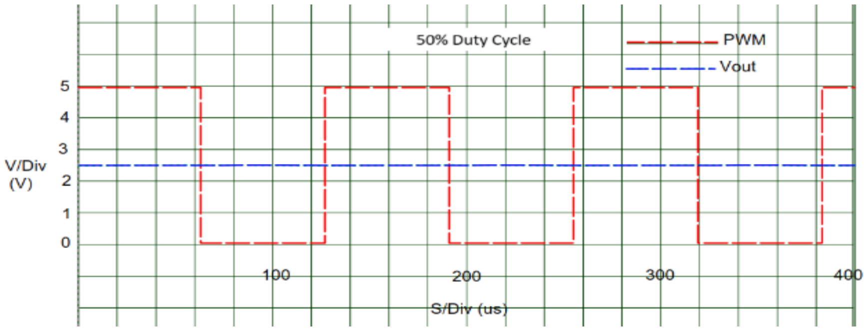

Fig 5. The PWM and the response of the simulation at 50% duty cycle.

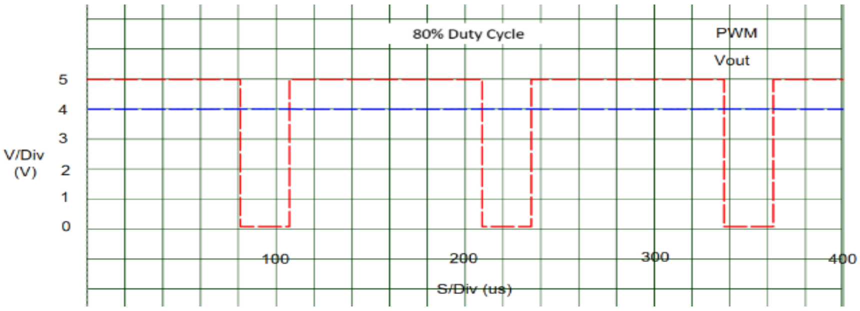

Fig 6. The PWM and the response of the simulation at 80% duty cycle.

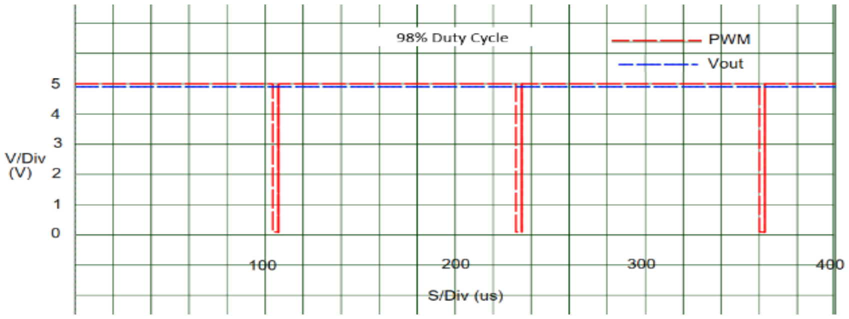

Fig 7. The PWM and the response of the simulation at 98% duty cycle.

5.2 Transient Response

Transient response refers to how a system reacts to a sudden change or disturbance before settling into its steady-state behavior (Bolton, , 2002). The observation for the settling time and load transient immunity for no-load is presented as follows:

5.2.1 Settling Time Measurement

The step response plot in Figure 9 (b) shows a settling time of less than 100ms under no-load conditions. This response plot from 0V to 2.5V (50% duty cycle) corresponds to 90% settling time.

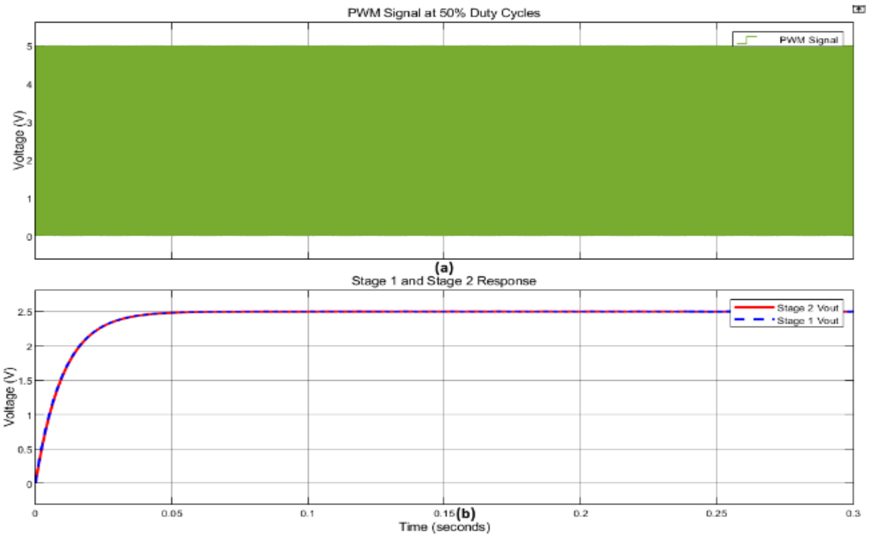

Fig 8. Settling time measurement for stage 1 and stage 2 RC low-pass filter.

6. LOAD TRANSIENT IMMUNITY

Load transient immunity is the capability of a system to sustain stable operation despite abrupt variations in load. In embedded systems and power electronics, it plays a vital role in ensuring consistent performance under dynamic conditions. (Wu, 2023; Kazi , 2019).

The system is connected to a load impedance of 10kΩ. The output stability under simulated load jumps and deviation is shown in Figure 10. The voltage deviation is 12.8% of V_{ref} during transients between the first-stage and second-stage filter.

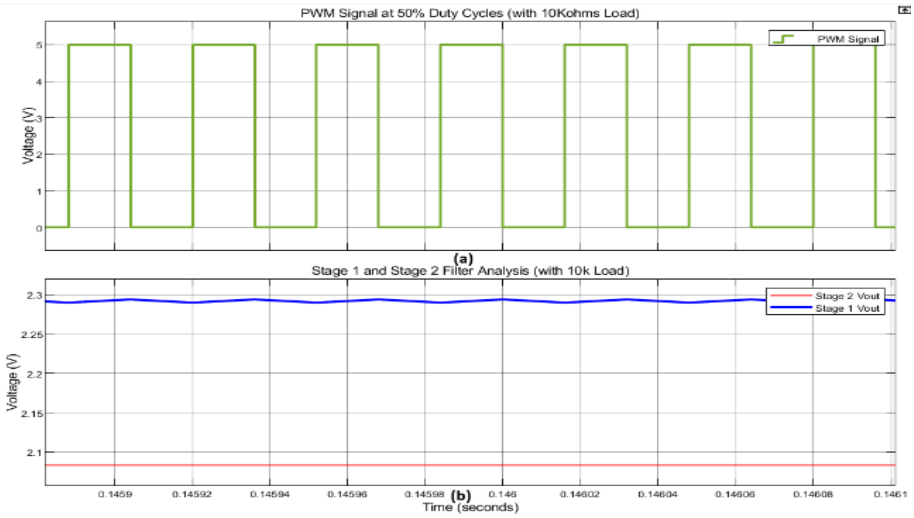

Fig 9. Load transient immunity at 10kΩ load impedance.

6.1 Filter Optimization Analysis

Filter optimization analysis in a second-order RC filtering circuit focuses on refining the circuit's performance by adjusting component values and configurations to achieve the best possible signal processing.

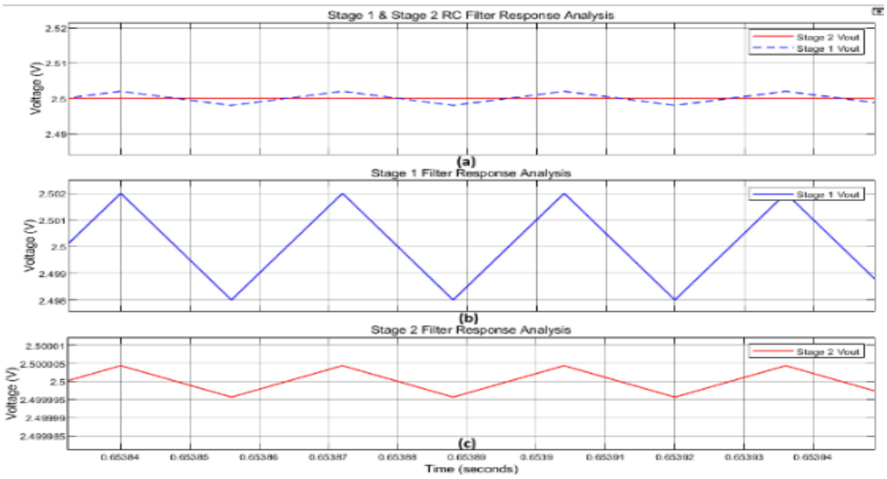

Fig 10. Simulation analysis of stage 1 and stage 2 RC low-pass filter comparison.

Second-order filters show steeper roll-off and better frequency selectivity compared to first-order filters as shown in Figure 11 (a). The stage one and stage 2 output voltage details are given in Figure 11 (b) and (c) respectively.

6.2 System Level Validation

System-level validation ensures that a system operates as expected, fulfilling its design specifications and performance requirements effectively. Table 3 and Figure 12 shows the simulated output of 5 set voltages. Table 3 observed the voltage reference, PWM signal, output voltage, and error computation.

Table 3. Voltage output validation of 5 voltage set measurement

Simulated Output of 5 Set Voltages			
Ref. Voltage	PWM (%)	Output ΔV_{out} (V)	Error (%)
1.0V	20	1.029	2.9
2.0V	42	2.014	0.7
3.5V	70	3.476	0.69
4.0V	80	3.974	0.65
4.7V	94	4.686	0.29

The voltage output response of the 5 selected reference voltage is simulated and the average error accuracy is listed in Table 3.

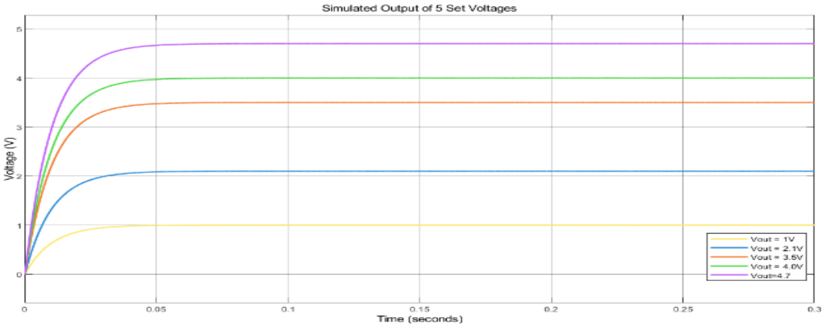

Fig 11. Simulation of the 5 selected reference voltages for computation of the accuracy error. The error is less than the 3% accuracy error from the targeted metric in section 2.5.

7. CONCLUSION

This study has demonstrated the successful design and simulation of a programmable Arduino-PWM-based reference voltage system for DC-DC converters using Proteus virtual prototyping. The simulation results validate that the implemented 10-bit PWM architecture with optimized two-stage RC filtering achieves precise voltage generation (0-5V range) with 4.88 mV resolution while maintaining excellent performance metrics including <1.5% output ripple and 70 ms settling time for full-scale transitions. The Proteus co-simulation environment proved particularly valuable in bridging digital control and analog circuit design, enabling comprehensive analysis of the PWM-to-analog conversion process and filter optimization prior to hardware implementation. Key findings include the 32% ripple reduction achieved through second-stage capacitor optimization and the system's cost-effectiveness, offering approximately 40% savings compared to commercial DAC solutions. The simulation-first approach developed in this work effectively reduces development iterations and provides a practical framework for power electronics researchers. Future work will focus on physical prototype validation, implementation of adaptive control algorithms for dynamic load conditions, and extension of the voltage range for broader applications. This research establishes a reliable methodology for developing programmable voltage references that balance performance and affordability, particularly beneficial for laboratory-scale DC-DC converter development and educational applications in power electronics.

8. ACKNOWLEDGEMENT

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